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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re The Application of:
Gilbert M. Wolrich et al.

Serial No.: 09/042,417

Filed: March 13, 1998

For: Reduction of Add-Pipe Logic by Operand Offset Shift

Examiner: Firmin Backer

Art Unit: 2155

Cesari and McKenna, LLP
88 Black Falcon Avenue
Boston, MA 02210
November 16, 2001

"Express Mail" Mailing-Label Number: EL 705606811 US

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

APPEAL BRIEF

Real Party Interest

The real party in interest is Compaq Computer Corporation. The inventors assigned their rights to Digital Equipment Corporation in an instrument recorded in the PTO on reel 9053, frame 001. Digital, in turn, merged into Compaq as set forth in a Cer-

tificate of Merger recorded against the above-identified patent application on Reel 11718, Frame 0409.

Related Appeals and Interferences

There are no other appeals or Interferences related to the patent application.

Status of Claims

The application was filed with claims 1-7, all of which are pending. Applicants are appealing from the rejection of all of these claims.

Status of Amendment

No amendments have been filed subsequent to the Final Rejection.

Summary of Invention

The invention relates to an adder/subtactor contained in a floating point unit of a microprocessor. Specifically it relates to normalization of the results of addition and subtraction operations of floating-point numbers.

A floating-point representation of a number includes (a) an exponent and (b) a mantissa that is multiplied by the exponent to arrive at non-floating point representation of the number. For example, in decimal notation the number 86,323 can be represented in floating-point format as $.86323 \times 10^{5}$. In a computer the floating point representation

includes bytes containing the mantissa and bytes containing the exponent. These include sign bits both for the exponent and for the overall number.

If two numbers have the same exponent they can be added merely by adding the mantissas. On the other hand, if the exponents are different, the mantissas must be aligned, a process in which the number with the smaller exponent is converted to a floating-point representation having the larger exponent. This involves subtracting the exponents and shifting the mantissa of the smaller number to the right by a number of bit positions equal to the difference in the two exponents.

Each processor has a standard format for the mantissas of floating-point numbers. For example, in Alpha microprocessors cited in the application, the most significant ONE bit in the mantissa is the bit immediately to the right of the binary point. Thus, the mantissa always has a value of at least one-half but less than one.

The addition of two mantissas may result in a sum that is greater than one, i.e., contains an ONE in the bit position immediately to the left of the binary point. In that case the result must be normalized to the standard format by shifting the mantissa one bit to the right and increasing the exponent by one. Conversely, a subtraction may result in a difference that is less than one-half, i.e., with a ZERO in the bit position immediately to the right of the binary point. In that case, the result must be shifted to the left by one bit and the exponent decreased by one. Normalization requires that the output circuitry of the adder be capable of a right-shift of one bit, a left-shift of one bit and no shift at all. The shifting is accomplished by means of a multiplexer which selects the connections

between its input lines and its output lines in accordance with the required shift (or no shift).

The invention operates to simplify the output multiplexer so that it selects among two shift possibilities instead of three. Specifically, whenever the adder is to effect an effective subtraction, that is, an addition of two numbers having different signs or a subtraction of two numbers having the same sign, the two inputs to the adder are shifted to the left by one bit as compared with the positions they would have if an addition were to take place. This is accomplished (a) by a means of a shifter 30 (Fig. 1; p. 4, l. 22-p. 5, l. 6) that is controlled to shift the larger mantissa one bit to the left when a subtraction is to take place, (b) and by causing an alignment shifter 32 to shift one fewer bit position to the right than it would if an addition were to take place. Accordingly, the mantissa resulting from a subtraction will be one bit to the left of the position it would otherwise have been.

Accordingly, no left-shift is required when the difference of two numbers would otherwise have left a ZERO in the bit position immediately to the right of the binary point. When that would not have been the result, the result is shifted to the right. Since shifting for normalization is accomplished by the multiplexers 188 and 164, the mutliplexers select among two positions, not three. They are thus less complicated and therefore faster (p. 25, l.15-20). The logic for rounding the results of addition and subtraction is also simplified (p. 25, l. 10-14; p. 26, l. 1-5).

Specifically, the output multiplexers can thus be capable only of two "shifts", namely, a right shift or no shift. This simplifies the construction of the output multiplexer and, furthermore, it speeds up its operation since there is a shorter path through the

circuitry that selects the multiplexer paths. The invention does require the addition of a multiplexer 30 (p. 5, l. 1-6). However, this is a simple multiplexer and, furthermore, its paths are selected during the operation of the alignment shifter. Its operation does not, therefore, affect the transit time through the adder.

Issue Presented

1. Whether the Lynch reference (U.S. Patent No. 5,901,076) discloses the concept of a shift to the left, prior to a subtraction, as compared with the positions the inputs would have if an addition were to take place.

2. The Examiner also rejected the claims for obviousness-type double patenting over claims in U.S. Patent 6, 018,756. The Applicants propose to file a terminal disclaimer obviating this rejection upon remand of the application, assuming reversal of the rejection based on the Lynch reference. Accordingly, double patenting is not an issue in this Appeal.

Grouping of Claims

Claims 1-7 were rejected on the same ground and accordingly there is a single group.

Argument

Claim 1, the only independent claim in the application defines a floating-point adder in which the novel feature described above is set forth in sub-paragraph B which states that

> "...for a least some pairs of mantissas, the mantissas signals applied to the main adder when the main adder is to subtract a pair of mantissas are off-

set to the left by one position from the mantissa signals applied thereto when the main adder is to add the same pair of mantissas."

According to the Examiner this feature is to be found in the Lynch patent. This reference relates to a floating-point adder, as does the invention at issue in this Appeal. Moreover, it relates to the alignment of mantissas of floating-point numbers which have different exponents. Specifically, it purports to speed up the alignment process by commencing the shifting of the mantissa having the smaller exponent before the subtraction of the exponents has been completed (see, e.g., Lynch, Abstract). The reference contains no suggestion that the mantissas be shifted differently prior to a subtraction operation than prior to an addition.

More specifically, the Examiner cites a number passages in the reference as disclosing the concept covered by the claims on appeal. We shall take these up in order.

The first reference is to column 1, lines 25-67. However this passage, along with the first 25 lines in column 2, describes a conventional floating-point adder/subtractor and, in particular describes the alignment process, in which the exponent of the number with the smaller exponent is increased by the difference between the exponents and the mantissa of the smaller number is shifted to the right a number of places equal to the exponent difference. There is no suggestion that the mantissa-shifting be changed in any way in order to deal with the normalization that may be required after an addition or subtraction operation.

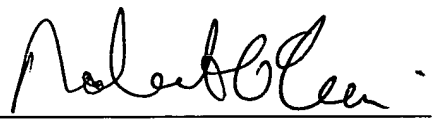
The next reference is unclear but it appears to begin on column 3, line 35 goes on to column 4, line 55. This passage describes the invention covered by the Lynch patent.

In particular, it describes an alignment arrangement in which the mantissa of the smaller number is right-shifted before the subtraction of exponents has been completed. There is no indication that the shifting is different for subtraction operation than for an addition.

The Examiner also cites column 6, lines 25-41 of the reference. This passage describes a second embodiment in which, rather than shifting the mantissa of the smaller number to the right the mantissa of the larger is shifted to the left by a number of places equaled to the difference between the two exponents. This, obviously will align the two numbers prior to addition/subtraction. However, there is no reference to a difference in the amount of shifting when the operation is a subtraction as opposed to addition.

Accordingly, the Lynch reference is entirely inapposite to the invention covered by the claims on Appeal. It does not disclose or even suggest the invention covered by the claims. We therefore request a reversal and remand of the application to the Examiner for subsequent entry of a terminal disclaimer and allowance of the application.

Respectfully submitted,



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APPENDIX TO APPEAL BRIEF

1. In a floating-point processor, an addition pipeline, adapted for application thereto of first and second operand signals, each of which represents the sign, exponent, and mantissa of a respective floating-point input operand, for performing an effective addition or subtraction on the input operands and generating an addition-pipeline output signal representing the result, the addition pipeline comprising:

A) a main mantissa adder adapted for application thereto of first and second processed mantissa signals and representing respective mantissa values, the main mantissa adder being operable selectively to perform addition and subtraction on the mantissa values and generate a mantissa-adder output, representative thereof, from which the addition pipeline generates the addition-pipeline output; and

B) mantissa-processing circuitry for so generating from respective ones of the input operands' mantissas and applying to the main mantissa adder respective processed mantissa signals that, for at least some pairs of mantissas, the mantissa signals applied to the main mantissa adder when the main mantissa adder is to subtract a pair of mantissas are offset to the left by one position from the mantissa signals applied thereto when the main mantissa adder is to add the same pair of mantissas.

2. An addition pipeline as defined in claim 1 wherein the main mantissa adder performs a normalization shift when necessary to produce an output within predetermined normalization limits but is capable of performing the normalization shift in only one direction..

3. An addition pipeline as defined in claim 2 wherein the main mantissa adder is capable of performing the normalization shift only to the right.

4. An addition pipeline as defined in claim 2 wherein the mantissa-processing circuitry comprises a pair of processing trains for generating first and second processed mantissa signals from respective input operands' mantissas, each processing train performing a shift, for at least a plurality of input-operand-value pairs, that is one more position to the left for an effective subtraction than for an effective addition.

5. An addition pipeline as defined in claim 2 wherein the main mantissa adder includes rounding circuitry operable in at least one rounding mode to add a rounding bit and being capable of adding the rounding bit at a selected one of only two bit positions in a given rounding mode.

6. An addition pipeline as defined in claim 1 wherein the main mantissa adder includes rounding circuitry operable in at least one rounding mode to add a rounding bit and being capable of adding the rounding bit at a selected one of only two bit positions in a given rounding mode.

7. An addition pipeline as defined in claim 1 wherein the mantissa-processing circuitry comprises a pair of processing trains for generating first and second processed mantissa signals from respective input operands' mantissas, each processing train performing a shift, for at least a plurality of input-operand-value pairs, that is one more position to the left for an effective subtraction than for an effective addition.